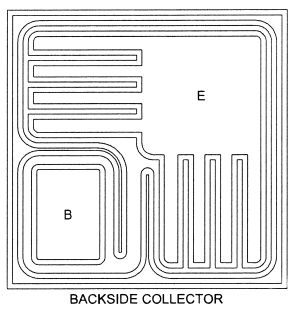
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



**.080”**

**.080”**

**Top Material: Al**

**Backside Material: Ti Pd Ag**

**Base = .018” X .027”**

**Emitter = .034” X .034”**

**Backside Potential: COLLECTOR**

**Mask Ref: CP230**

**APPROVED BY: DK DIE SIZE .080” X .080” DATE: 11/17/21**

**MFG: CENTRAL SEMI THICKNESS .008” P/N: 2N6039**

**DG 10.1.2**

#### Rev B, 7/19/02